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Xeons L3 cache

Options

bronx

Registered User
Posts: 0
Member Since: 11-25-2002

Posted: 07-23-2003 10:46 AM ID#: 146 (Viewed 595 times)

The launch of the Xeon 3.06 w/1MB L3 at an affordable price point has attracted the interest of the developer community to the L3 cache potential. At the moment, there is some confusion it seems concerning the behavior of this L3 cache. I've read on some forums people saying things like "the L3 is exclusive with 100% certainty" and others arguing that on the contrary it's purely inclusive with the L2. Any clarification on the matter will be welcome. I know it's slightly OT but I don't know where else to ask.

Some basic questions :

I) In the Xeon 3.06 w/1MB L3, the L3 - L2 relation is :

- (a) mostly exclusive
- (b) mostly inclusive
- (c) too complex to be described
- (d) a trade secret

II) If we compare the L3 cache behavior of the Xeons 3.06 w/1MB L3 and the latest Xeons MP with 1MB L3, we can say it is :

- (a) 100% the same
- (b) mostly the same with small differences
- (c) completely different
- (d) this information isn't disclosed

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Re: Xeons L3 cache

Options

ShuoL

Registered User
Posts: 0
Member Since: 04-25-2003

Posted: 07-29-2003 03:03 PM ID#: 147 (Viewed 594 times)

The short answers to your questions are b) and a) Let's not forget that 1) there are tremendous benefit in having a on-die level 3 cache. 2)Both Level 3 Cache designs are full speed, 8-way associative with ECC capability.

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Re: Xeons L3 cache

Options

bronx

Registered User
Posts: 0
Member Since: 11-25-2002

Posted: 07-30-2003 02:56 AM ID#: 148 (Viewed 594 times)

thanks a lot for your answer

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